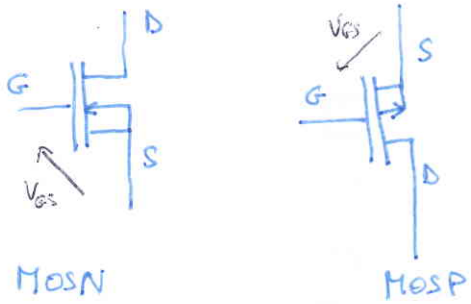
Transistors MOS : MOS : Metal Oxyde Semi-Conductor

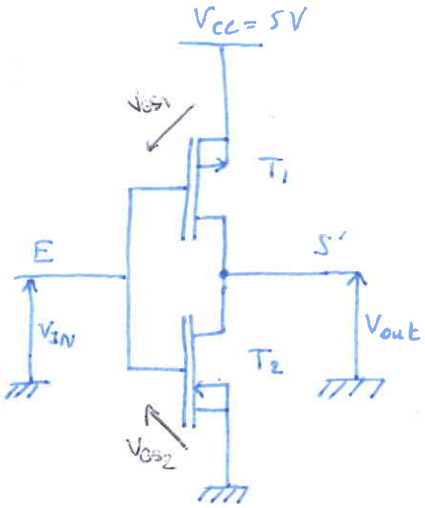


MOSN : Bloqué si $V_{GS} = 0V$
Conducteur si $V_{GS} = 5V$

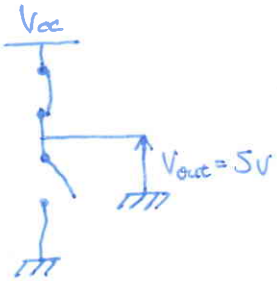
MOSP : Bloqué si $V_{GS} = 0V$
Conducteur si $V_{GS} = -5V$

[Mémo technique :
MOSP → la flèche Part
MOSN → la flèche Ne peut pas.]

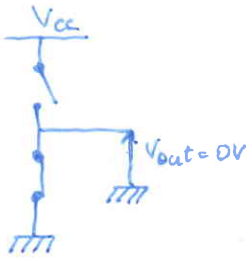
Portes logiques en technologie CMOS : CMOS : Complementary MOS



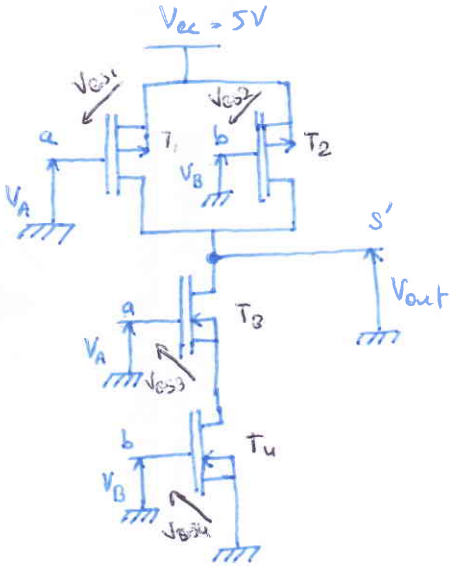
- $V_{IN} = 0V$:
  - $V_{GS_1} = 0 - V_{cc} = -5V \Rightarrow T_1$ conducteur
  - $V_{GS2} = 0 - 0 = 0V \Rightarrow T_2$ Bloqué



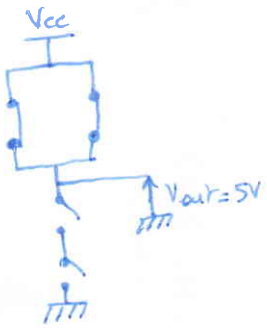
- $V_{IN} = 5V$:
  - $V_{GS_1} = 5 - V_{cc} = 0V \Rightarrow T_1$ Bloqué
  - $V_{GS_2} = 5 - 0 = 5V \Rightarrow T_2$ Conducteur



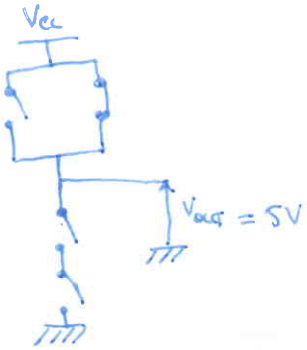
C'est une porte NON



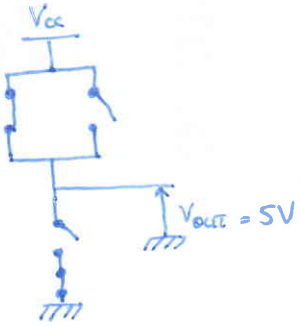
- $V_A = 0V$ et $V_B = 0V$:
  - $V_{GS1} = 0 - V_{cc} = -5V \Rightarrow T_1$ Conducteur
  - $V_{GS2} = 0 - V_{cc} = -5V \Rightarrow T_2$ Conducteur
  - $V_{GS3} = 0 - 0 = 0V \Rightarrow T_3$ Bloqué
  - $V_{GS4} = 0 - 0 = 0V \Rightarrow T_4$ Bloqué



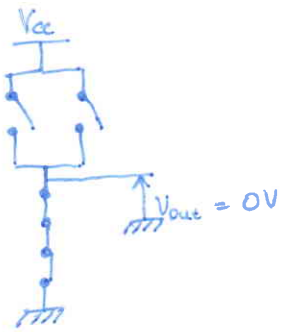
- $V_A = 5V$ et $V_B = 0V$:
  - $V_{GS1} = 5 - V_{cc} = 0V \Rightarrow T_1$ Bloqué
  - $V_{GS2} = 0 - V_{cc} = -5V \Rightarrow T_2$ conducteur
  - On ne peut pas calculer V_{GS3}
  - $V_{GS4} = 0 - 0 = 0V \Rightarrow T_4$ Bloqué



- $V_A = 0V$ et $V_B = 5V$:
  - $V_{GS1} = 0 - V_{cc} = -5V \Rightarrow T_1$ Conducteur
  - $V_{GS2} = 5 - V_{cc} = 0V \Rightarrow T_2$ Bloqué
  - $V_{GS3} = 0 - 0 = 0V \Rightarrow T_3$ Bloqué
  - $V_{GS4} = 5 - 0 = 5V \Rightarrow T_4$ Conducteur



- $V_A = 5V$ et $V_B = 5V$:
  - $V_{GS1} = 5 - V_{cc} = 0V \Rightarrow T_1$ Bloqué
  - $V_{GS2} = 5 - V_{cc} = 0V \Rightarrow T_2$ Bloqué
  - $V_{GS3} = 5 - 0 = 5V \Rightarrow T_3$ Conducteur
  - $V_{GS4} = 5 - 0 = 5V \Rightarrow T_4$ Conducteur



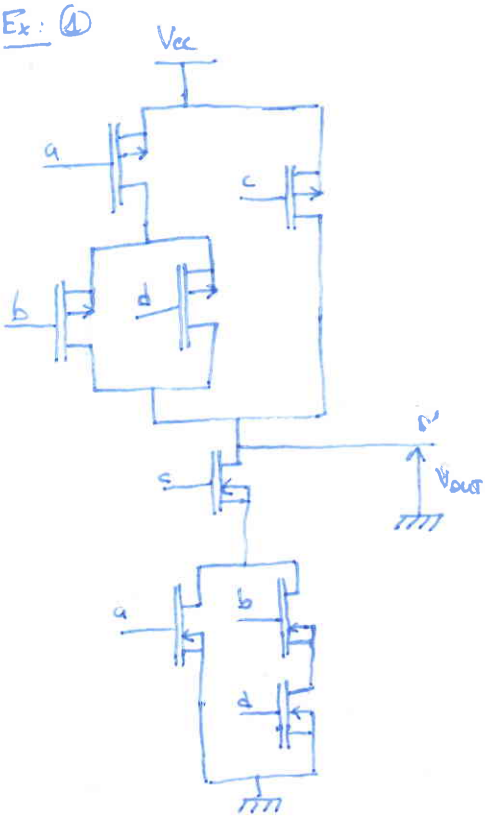
E_A	E_B	S
0	0	1
1	0	1
0	1	1
1	1	0

Porte NON-ET
NAND

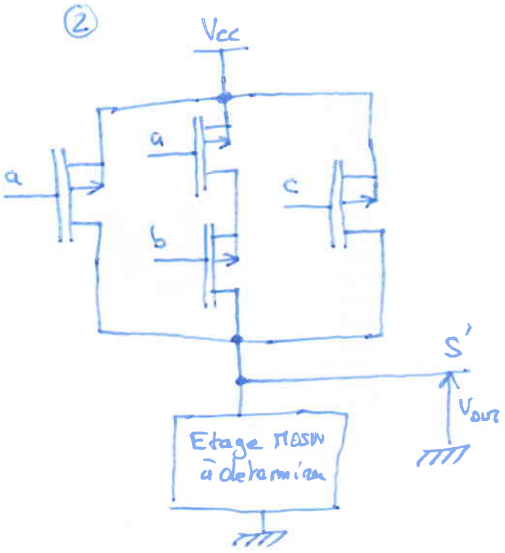
$T_1 // T_2$
$T_3 + T_4$ ⇒ Complémentarité

$V_{OUT} = V_{cc}$ si (T_1 Cond) ou (T_2 Cond)
si ($V_{GS1} = -5V$) ou ($V_{GS2} = -5V$)
si ($V_A = 0V$) ou ($V_B = 0V$)
si ($a = 0$) ou ($b = 0$)
$S' = \bar{a} + \bar{b} = \overline{a.b}$

Ex : ①

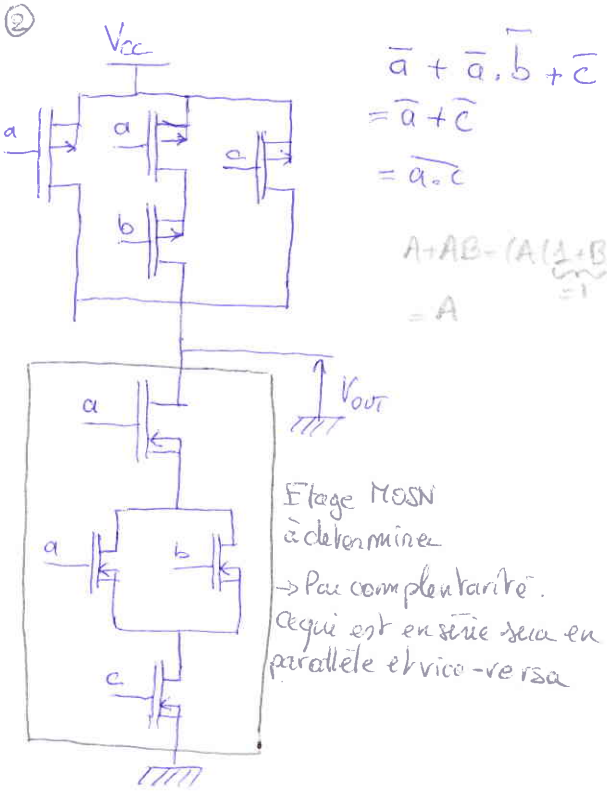


②



Fonction logique en tech CMOS
1) Equation logique
2) Simplification de l'équat° du ①
3) Schéma complet simplifié

(2)



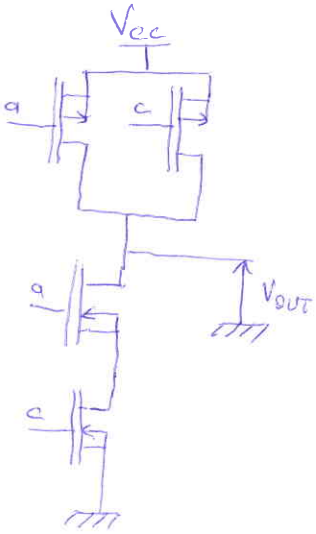
$\bar{a} + \bar{a}.\bar{b} + \bar{c}$

$= \bar{a} + \bar{c}$

$= \overline{a.c}$

$A + AB = A(1 + B)$ ($1 + B = 1$)

$= A$

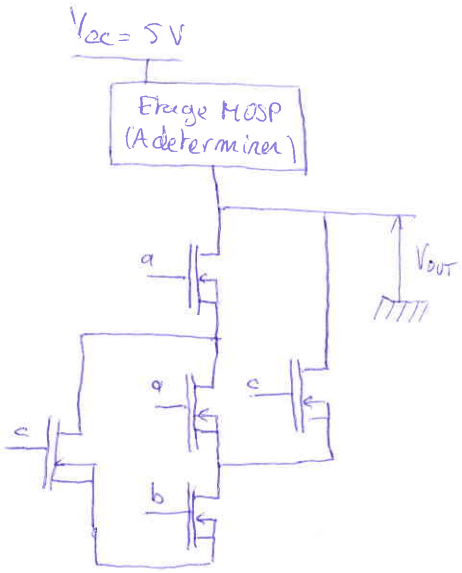


Etage MOSN à déterminer

→ Pas complémentaire.

Ce qui est en série sera en parallèle et vice-versa

(3)



$\bar{S} = (a.(c + (a.b))) + (b.c)$

$S = (\bar{a} + (\bar{c}.(\bar{a} + \bar{b}))).(\bar{b} + \bar{c})$

$S = (\bar{a} + (\bar{c}\bar{a} + \bar{c}\bar{b})).(\bar{b} + \bar{c})$

$S = \bar{a}\bar{b} + \bar{a}\bar{c} + \bar{b}(\bar{c}\bar{a} + \bar{c}\bar{b}) + \bar{c}(\bar{c}\bar{a} + \bar{c}\bar{b})$

$S = \bar{a}\bar{b} + \bar{a}\bar{c} + \bar{b}\bar{c}\bar{a} + \bar{b}\bar{c} + \bar{c}\bar{a} + \bar{c}\bar{b}$

$S = \bar{a}\bar{b} + \bar{a}\bar{c} + \bar{b}\bar{c}$

$S = \bar{a}(\bar{b} + \bar{c}) + \bar{b}\bar{c}$